Phase Locking the IPNS Neutron Choppers to the 60 Hz Power Line*

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Introduction

The neutron beam chopper is a cylinder made of a neutron absorbing material with slits which permit neutrons to pass through. The revolution frequency (typically 270 revolutions per second) and the width and curvature of the slits determines the range of energies that can be transmitted to the experimental sample. The time from when neutrons are released from the pulsed neutron source to the alignment of the slits to permit passage of neutrons determines the energy of neutrons that will be passed by the chopper. The chopper operates in a partial vacuum and is rotated by a fractional horse power synchronous motor. The chopper rotates at a frequency multiple of 30 Hz. Several of the neutron scattering instruments at the Intense Pulsed Neutron Source (IPNS) at Argonne National Laboratory (ANL) use neutron choppers to select the energy of the neutron beam required for their experiment. Since the neutron burst is generated by the 100 ns proton beam extracted from the Rapid Cycling Synchrotron (RCS), precise synchronization must be maintained between the RCS extraction and the chopper slits. To accomplish this, a chopper rotor position signal is used to generate the RCS extraction pulse; therefore, the RCS must be synchronized to the chopper. The chopper master clock generates a 30 Hz reference signal that is used by both the RCS and chopper controllers for synchronization. The RCS operates at 30 Hz and performs best when synchronized to the 60 Hz power line. This paper describes equipment required to synchronize a chopper to the power line.

60 Hz Line Synchronizaton Requirements

Through operating observations it has been determined that the RCS performance increases as the RCS pulse rate approaches one half the 60 Hz power line frequency. Performance continues to improve as phase excursions are limited down to $\pm 15^{\circ}$, after which further tighter phase control is not expected to greatly improve RCS performance. Except for short periods of time the power line frequency ranges from 59.95 Hz to 60.05 Hz.

Rotor Stability Requirements

When more than one chopper is operating, one is denoted as the master chopper, the rest are slave choppers. A rotor position signal from the master chopper is used to produce an extraction master pulse (EXM) resulting in beam being extracted from the RCS. The slave choppers must rely on being precisely synchronized to the master chopper to determine energy resolution. TC is the time from when the proton beam arrives at the target and a chopper rotor position signal. If ΔTC is outside limits (typically ± 1.0 μs for a master and ± 2.0 μs for a slave, the data from the instrument will not be taken. Because of the method used to make phase corrections, the choppers may not be operating in the center of ΔTC. This further tightens the requirements on rotor stability. To maintain good data taking rates and high energy resolution from the chopper instruments, the rotor must maintain a phase stability to the master clock 30 Hz reference of ± 1.0 μs (approximately equal ± 0.1 degrees of rotation).

RCS Chopper System Description

For the purpose of this paper a detailed understanding of how the chopper and the RCS are phased locked to each other is not necessary. It is only necessary to know that they both have phase control systems that seek to properly phase them with the 30 Hz reference from the master clock (Fig. 1). The Variable Frequency Master Clock (VFMC) has the ability to phase lock the 30 Hz reference to the 60 Hz power line. In response to the chopper controller, the frequency synthesizer produces chopper motor drive signals properly phased to produce the correct dynamic rotor position with respect to the 30 Hz reference. By measuring the period of the magnetic pickup the damper can detect positive or negative acceleration of the chopper rotor. The damper then phase shifts the motor drive signal in a direction to reduce the acceleration. The current regulator and power amplifier supplies a steady current to the motor windings in response to the drive signals.

The chopper controller system has several functions of which only the generation of a EXM and delayed 30 Hz are relevant to this discussion. After a programmable delay from the magnetic pickup, the EXM is generated. The amount of delay is calculated by the chopper controller to produce the desired neutron energy based on the time from EXM to beam arriving at the uranium target, chopper period, and the phase relationship between the magnetic pickup and the slits on the chopper rotor. A second programmable delay from the 30 Hz reference generates a delayed 30 Hz which causes the frequency synthesizer to position the chopper rotor so the proton beam will be extracted from the RCS at a preset phase of the 30 Hz reference.

The RCS controller synchronizes the RCS so that beam can be extracted from the RCS at a preset phase of the 30 Hz reference and generates an EXM acceptance window at that time.[1]

The three changes that were required to allow the chopper system to follow the 60 Hz power line are: 1) to make the master clock into a variable frequency master clock, 2) add chopper dampers to improve chopper rotor stability, and 3) update the chopper controller system to maintain monochromatic neutron beam as chopper period is changed. The purpose of this paper is to describe the circuitry of the VFMC and the chopper damper.[2]

Variable Frequency Master Clock Circuit Description

The VFMC contains a voltage controlled crystal oscillator (VCXO) with a center frequency of 3.93216 MHz (referred to as 4 MHz C). The 4 MHz C is divided by 2^{16} to get the 60 Hz clock (referred to as 60 Hz C). The 60 Hz C is divided by 2 (Fig. 2) to get 30 Hz clock (30 Hz reference). If the 60 Hz C is to be phase locked to the 60 Hz power line the 60 Hz C must have a frequency range that encompass the frequency range of the 60 Hz power line. Observations of the power line frequency at ANL reveal that a range from 59.95 Hz to 60.05 Hz would be sufficient for our purpose. From this the frequency range requirements for the 4 MHz C can be calculated:

$$\text{Minimum frequency} = 59.95 \text{ Hz} \times 2^{16} = 3.92888 \text{ MHz}$$

$$\text{Maximum frequency} = 60.05 \text{ Hz} \times 2^{16} = 3.93544 \text{ MHz}.$$

The VCXO is programmed to cover this frequency range by the output of a 12 bit digital to analog converter (D to A). This provides a method of programming the frequency between minimum frequency and maximum frequency in 2^{12} (4096) bits. The frequency change for each bit can then be approximated as

Frequency maximum - frequency minimum/4096 x frequency center=

$$3.93544 \times 10^6 - 3.92888 \times 10^6/4096 \times 3.93216 \times 10^6 = 1/2.46 \times 10^6$$

or one bit equals a change of one part in 2.4×10^6. This provides adequately small and predictable step changes for the chopper rotor to follow without creating rotor instability.

The output of a 12 bit up/down counter referred to in Fig. 2 as frequency register is connected to the D to A. This provides a method for stepping the input to the D to A up or down. The restrictions on stepping the frequency register are to step at a rate no faster than the chopper rotor can follow, and not to let the frequency register roll over (go higher than 2^{12} or lower than zero) and a correction must be required in the frequency of the VCXO. The parameters that determine if the frequency register needs to be changed are derived from comparing the 60 Hz C along with its source the 4 MHz C and the 60 Hz power line. A 60 Hz band pass filter and a zero crossing detector are used to get a low noise signal (60 Hz L) that represents the 60 Hz power line. If the 60 Hz C and 60 Hz L are correctly phased then the proper frequency for the VCXO is (60 Hz L) x 2^{16}. If phase correction is required then the proper frequency for the VCXO is (60Hz L) x (2^{16}) $\pm(\Delta F)$ when ΔF represents the frequency shift used to cause the phase correction.

The programmer and the cycle counter count all of the cycles of the 4 MHz C that occur in the period of one cycle of 60 Hz L. The phase comparator supplied the cycle counter with the 12 least significant bits of the number 2^{16} - K $\pm(\Delta F)$ where K is the number of cycles counted by the programmer. A comparison is made between the number supplied by the phase comparator and the number of cycles counted by the cycle counter. If the two are unequal the results are passed on to the frequency controller as an enable up count or enable down count.

The magnitude comparator compares the output of the frequency register to adjustable limits. If the frequency register is larger than the upper limit, the up count is disabled in the frequency controller. If the frequency register is smaller than the lower limit, the down count is disabled.

If the up count or the down count has not been disabled by the cycle counter of the magnitude comparator then the frequency controller activates the corresponding count input to the frequency register when the frequency controller is strobed. Up counts and down counts are also distributed outside the VFMC for use in chopper damper circuitry.

The strobe is adjustable from 0.5 Hz to 60 Hz allowing the frequency register to be updated at a rate that the chopper rotor can follow. The functions of the programmer are to activate the strobe and reset the cycle counter, phase comparator, and selector. The selector sends the 4 MHz C to the programmer when it is set by the 60 Hz L. After being reset by the programmer the selector sends the 4 MHz C to the cycle counter.

Neutron Chopper Damper Theory of Operation

The chopper rotor is driven by a hysterises synchronous motor. As indicated by Fig. 3, the rotor would lag the stator magnetic axis by the stable rotor load angle. Within limits, as rotor load angle increases, motor torque increases. When the rotor velocity is changed it causes a change in instantaneous rotor load angle. Without damping, the instantaneous rotor load angle would oscillate about the stable rotor load angle. The phase shift amplifier has the ability to shift the stator magnetic axis. The damper measures changes in rotor velocity to generate an error signal to control the phase shift amplifier. When the rotor is accelerating, the phase shift amplifiers shift the stator magnetic axis in a direction to reduce the instantaneous rotor load angle. This reduces motor torque and acceleration.

Chopper Damper Circuit Description

The chopper period is measured by gating a 100 MHz clock into the accumulator (Fig. 4) for 28 revolutions of the chopper. A change in chopper period of approximately 1 part in 10^7 would cause the resultant number in the

accumulator to change by 1. The number in the accumulator is saved in the D to A register whose output is converted to analog by the D to A converter and is used as an error signal. The error signal is added to other correcting signals and used as phase control by the phase shift amplifiers. To keep the D to A converter operating in the center of its control range, the accumulator is preset to the value in the offset register. The D to A register is checked by the offset detector to see if it is in the midrange of the D to A converter. If it is not, the offset register is incremented or decremented in the direction to put the D to A converter in midrange. When the VFMC changes frequency, the chopper period will have to change. Without additional inputs the damper would try to prevent the chopper period change. The accelerator, responding to up or down counts from the VFMC, adjusts the offset register, so when the chopper reaches its new period, the D to A converter will be in midrange. To calculate the amount of change in the offset register note that when the VFMC frequency register is changed by one count the 4 MHz C changes by one part in 2.4×10^6. This will cause the same change in the chopper period. The calculation of the change in accumulator counts is then

28 revolutions x chopper period x clock rate x one part in 2.4×10^6 parts =

$28 \times (1/270) \times 100 \times 10^6/2.4 \times 10^6 = 4.3$.

Therefore, if a up count is received from the VFMC the accelerator would increase the number in the offset register by 4 counts. The accelerator also puts an offset into the error signal summing amplifier for a short time to help get the chopper to its new period faster. When the starter detects the 28 revolutions of the chopper, it sets the set reset. This action results in gating the 100 MHz clock to the accumulator off and on to the timer and programmer. The amount of time measured by the timer plus the amount of time measured by the accumulator is 28 times the chopper period. The timer measures a precise amount of time for the programmer to operate before resetting the set reset. The programmer loads the D to A register from the accumulator, updates the offset register,and loads the offset register into the accumulator.

Damper Tests and System Operation

In order to test the damper, the chopper drive signal period was increased to cause the chopper period to increase by 89 ns. This change was introduced linearly over 2 s (Fig. 5 - upper trace). The three time frames represent three conditions: 1) no active damping in circuit, 2) active damping added to circuit and 3) the addition of the accelerator function to the active damper. On June 13, 1985, the IPNS started operating on the VFMC with the VFMC tracking the 60 Hz power line. During the first seven days of operation, one master chopper and one slave chopper were operating. The master took data 99.4% of the time and the slave took data 98.8% of the time. This is within the range of efficiencies that would be normal if the IPNS were operating on a fixed clock. The 30 Hz reference has been between $\pm 40^0$ of the desired power line phase 96% of the time. Tests indicate that there would be little effect on chopper stability and data taking efficiencies if the VFMC were set to more tightly follow the 60 Hz power line. Measurements were taken of energy resolution of the neutron beam passed by the choppers while the IPNS was operating on a fixed clock and the VFMC. The measurements did not show any change in the energy resolution.[2] The purpose of operating the IPNS on the VFMC was to improve the intensity and stability of the proton beam in the IPNS. The beam current for the seven days of operation before the VFMC was installed was 11.70 μa. After the operators had been tuning on the line locked IPNS for four days, the average beam current was above 13 μa. The average current for the next four days was 13.63 μa. Other changes were made at the same time the VFMC was installed and it is not known how much each contributed to the increased beam current, but it is believed that the most significant gain came from operating the IPNS locked to the power line.

Acknowledgements

References

[1] A. Rauchas, et al., "IPNS Accelerator System and Neutron Chopper Synchronization," Proceedings of International Collaboration on Advanced Neutron Sources (ICANS-VII), Atomic Energy of Canada Limited, Report AECL-8488 (Sept. 13-16, 1983) 157.

[2] G. E. Ostrowski, et al., "The IPNS Chopper Control and Accelerator Interface Systems," proceedings of this conference.
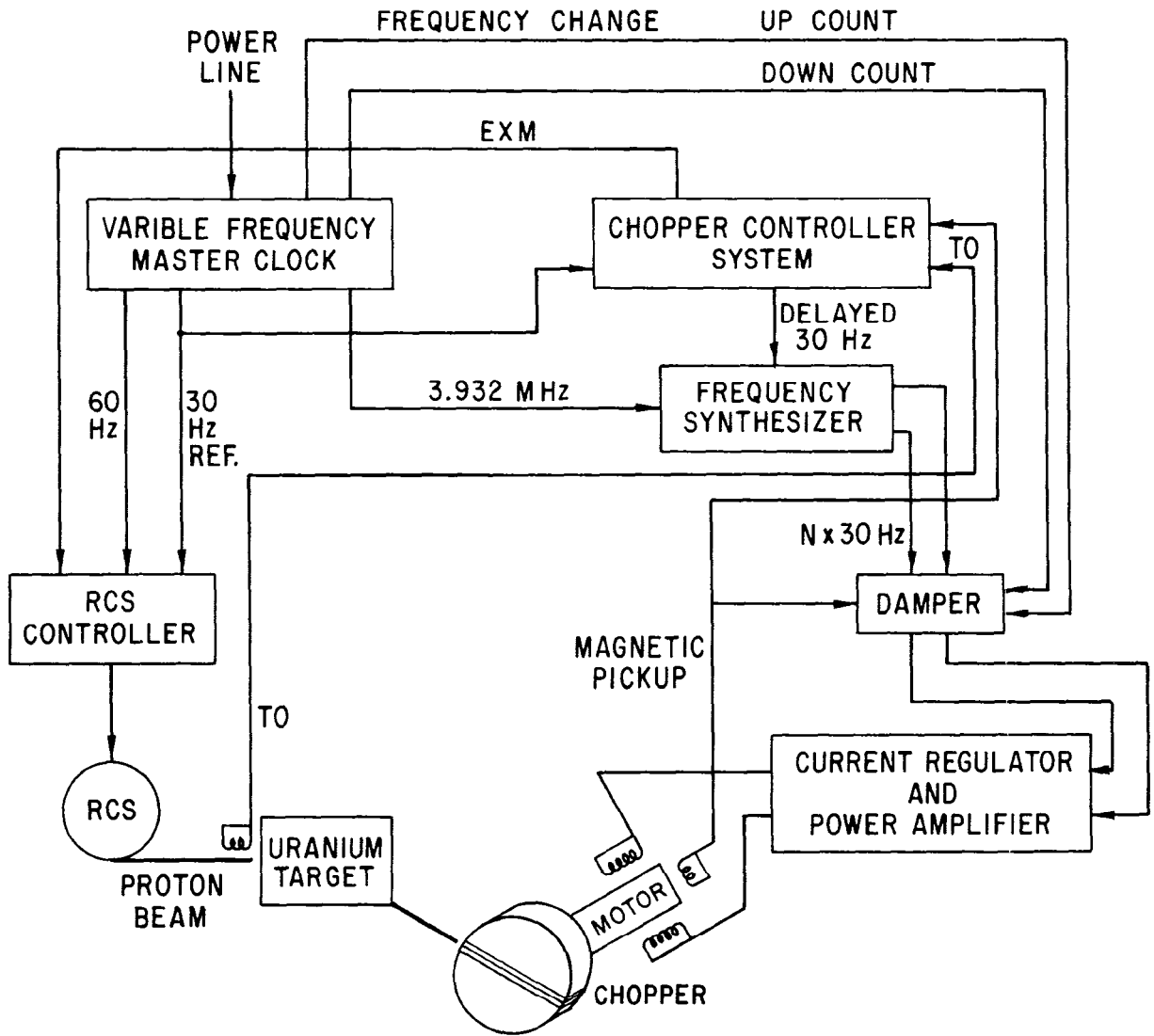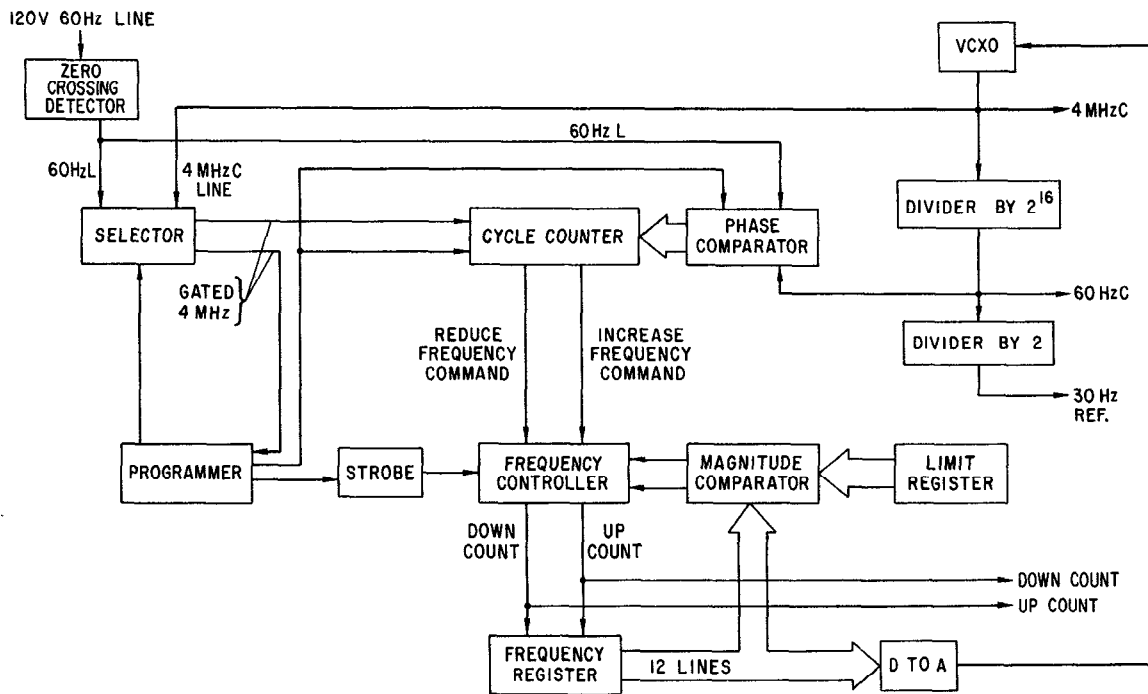
Fig. 1. Chopper IPNS control system.

Fig. 2. Variable frequency master clock.

PHASE SHIFT IN STATOR MAGNETIC AXIS DUE TO PHASE SHIFT AMPLIFIER
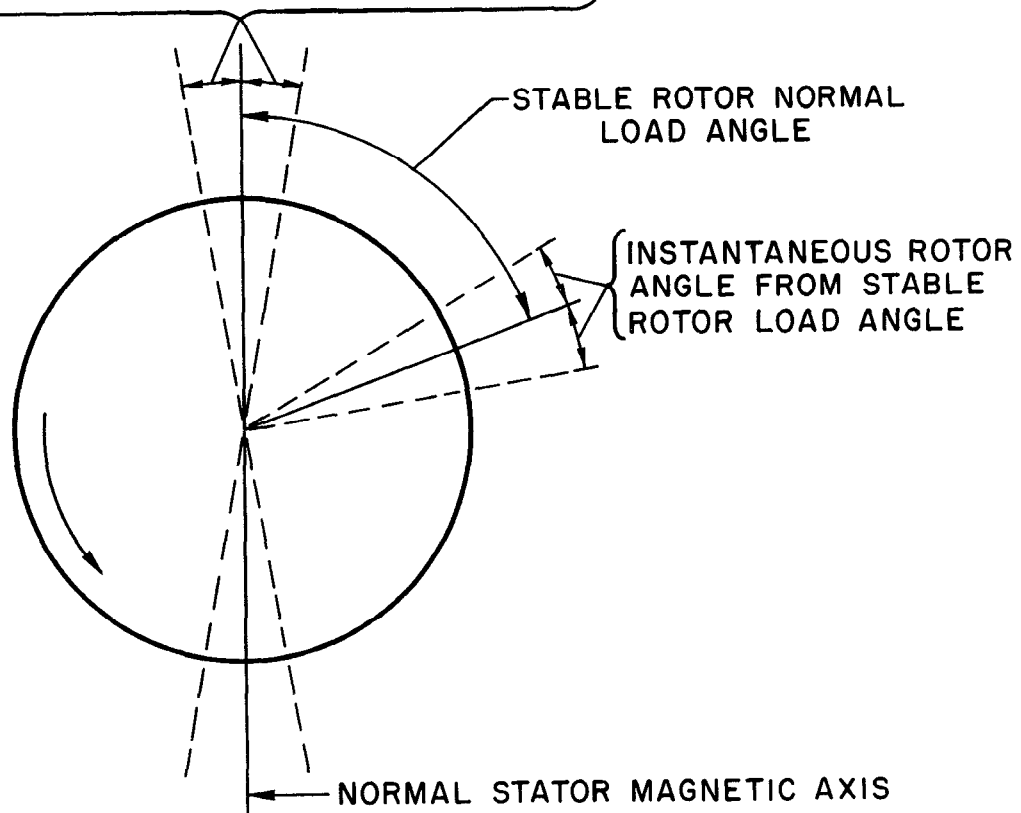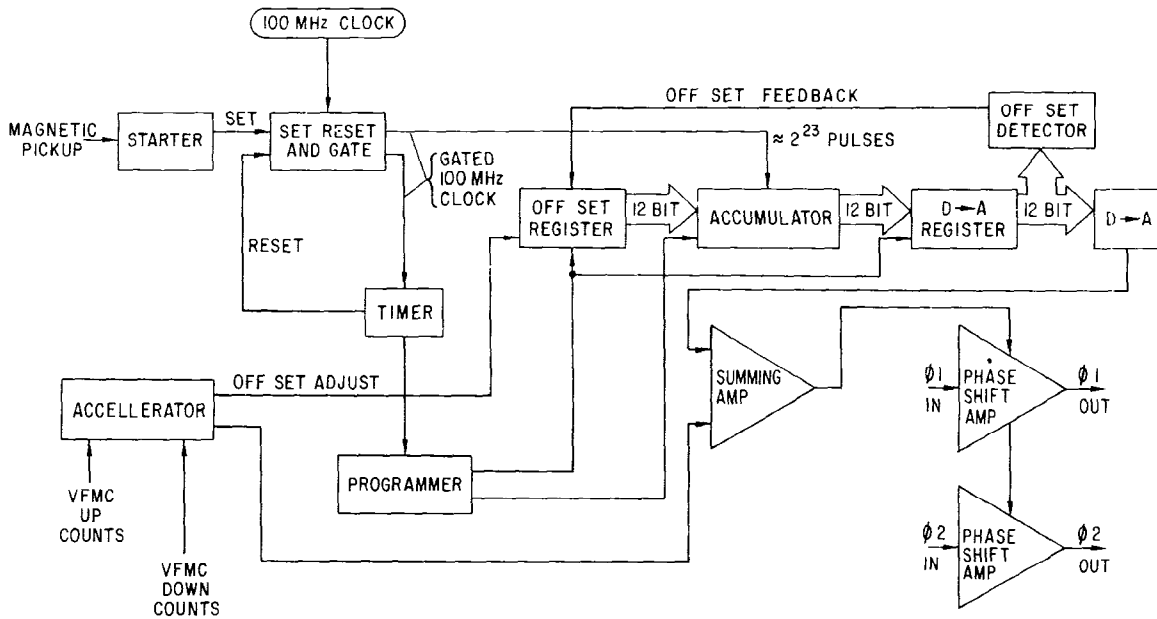

Fig. 3. Rotor load angle.
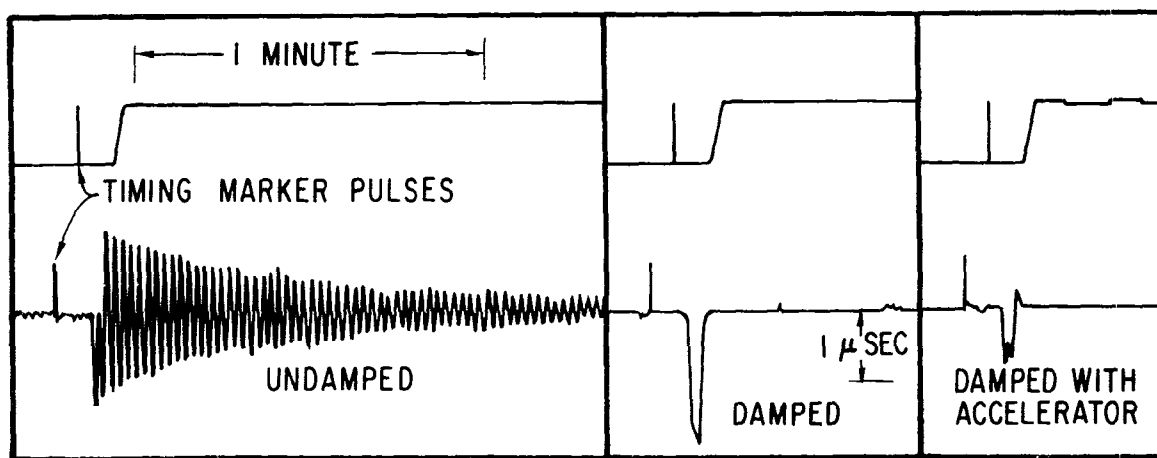
Fig. 4.   Active chopper damper.

Fig. 5.   Strip chart.