Data Acquisition and Analysis Systems on SNS

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1 Introduction

The whole system has been give" the acronym PUNCH: PUlsed Neutron Computer Hierachy.

The PUNCH system will be organised at four levels:

i) The data acquisition electronics (DAE) at each instrument will record the arrival of each detected neutron by incrementing the appropriate word in a memory whose size is determined by the required number of space-time channels. Prototypes of this level have already bee" built in the Rutherford Laboratory's Instrumentation Division.

ii) Each neutron instrument will have its own front-end minicomputer (FEM) to control the course of the experiment and to collect the data. Its

iii) The FEMs will all be linked to a single, medium sized RUB computer having a large disk data base (2 - 3 Gbytes), capable of storing some 2 - 3 weeks of experimental data as well as programs. The HUB

iv) Tbe RUB computer will be linked to the Rutherford Laboratory main-frame computers and hence to remote stations via the SRC network.

Figure 1 Illustrates the four-level hierachy described above.

A simple prototype of an external memory incrementing DAR system coupled to a PDP11/34 has been built and tested. It awaits field trials on the Harwell linac.

A detailed design of the SNS DAE is in progress and is described below.

A hardware/software specification for the FEM/HUB computers has bee" drawn up and circulated to 21 manufacturers (Nov '79), in a pre-tender exercise. Ten manufacturers responded. A very brief summary of this specification is included below under the headings FEM. ROB and Communications. Since

2 Data Acquisition Electronics

The DAE is being designed by the Instrumentation Division at the Rutherford Laboratory and is shown in Figure 2. It consists of up to 16 TOF crates and a system crate. Bach TOF crate contains up to 23 TOF modules and a crate control module.

Each TOF module houses two separate channels. A channel may be fed by a single detector or a number of detectors via a position encoder module. I" the latter case positional information is passed to the module via a front panel connector. When an event occurs on one of these detectors the appropriate space (from the detector) and time (from the TOF bus) information is stored in one of the dual 256 wd memory buffers located in each channel ('DUAL BUFF' in Figure 2a). Thus during a neutron frame (20 ms on SNS) one of the dual buffers is filled while the other is being read (via the data section of the TOF bus). The fact that all of the information for one frame is stored in the TOF module before being incorporated in the bulk memory means that it may be verified before transmission. If any of the error conditions are set (eg due to an overflow in a dual memory buffer) the frame is not read and the 'frame-lost' counter incremented.

The output from a single detector or a position encoder module may also be splayed (via a splay module) to two or more TOF modules. Using the splay technique the effective depth of the dual memory buffers may be increased in units of 256 wds. From each TOF crate the information stored during the previous frame is read out via the instrument bus to the systems crate. Within the crate the instrument bus interface introduces the frame counter information (used in experiments studying relaxation phenomena) resulting in a total of 41 bits of information being presented to the descriptor generator. This is reduced in two stages. A hardware patch removes those bits which are redundant for all experiments on the particular instrument. Secondly a programable section (show" as the ROM and COMPACTOR in Figure 2b) produces the compacted descriptor in a manner that may be tailored to each experiment. This, final, descriptor is the" passed to the bulk store via a" INTEL multibus to effect a Read Increment-Write (RIW) cycle on the appropriate address.

The FEM will be connected, via a suitable interface, to the Intel multibus for DMA transfer of the Bulk store contents to the FEM memory (not show" in figure 2).

3 Front-End Minicomputer

Hardware Configuration

CPU + optional hardware multiply/divide.

OS + 80 Kbyte of < 1 μs main memory

Hardware bootstrap and programmer's console.
20 Mbyte of disk storage which at least 2 Mbyte must be demountable.
Inexpensive hardcopy alphanumeric terminal.
Interactive graphics terminal (ie with graphics cursor facilities).
> 5 Kbyte/s serial synchronous interface to HUB or communications computer.
BUS interface supplied by the Rutherford Laboratory.
CAMAC crate controller.

4 FEM Software

i) The operating system. The minimum requirements of the operating system are to permit two real-time tasks to execute in conjunction with the network software. The OS could be single-user.

ii) The network software. This should permit remote log-in to the HUB from FEM terminals and file transfer facilities. It should be possible to initiate file transfer by terminal commands or under program control.

iii) Applications software PEANO for experiment control

iv) Application software DEDEKIND for data display

vi) Other specialist applications software will deal with subsequent data treatment.

5 HUB and Workstation

Hardware Configuration

32 bit (or larger) word CPU and ancillary hardware such as cache and hardware floating point unit to provide 0.2 IBM 360/195 equivalent processor.
Operator's console and VDU.
1 Mbyte of main memory which can be expanded to at least 2 Mbyte.
2 Gbyte of disk storage which can be expandable to 3 Gbyte.
600 lpm line printer.
3 x 6250 bpi tape drives.
Interface(s) for network connections from FEM's and RLM or communications computers.
Interfaces to HUB workstations.

Two HUB workstations. Each will comprise:

i) workstation control processor and suitable communications interface(s);

ii) 10 x interactive graphics terminals with graphics cursor facilities. These "nits should be identical to those on the FEMs. Shared hardcopy facilities are necessary;

iii) 600 lpm line printer;

iv) High speed, high quality hardcopy graphics plotter;

v) a demountable cartridge disk drive or floppy drive, of the same type as used on the FEM computers. This device is required on one workstation only.

6 HUB Software

operating system

A virtual, multi-user, multi-tasking operating system should provide the following facilities:

Up to 30 simultaneous, logged-on users. It is expected that ∿ 40% of these users will be executing existing data reduction programs requiring a high floating arithmetic activity.

A further ∿ 40% will be viewing/editing their data "sing the interactive graphics terminals and obtaining hardcopy graphics output.

The remainder will be developing new programs (compiling, editing, linking etc).

In addition to the logged-on users there will be continual file transfer from all the FEMs to the HUB (at a mean rate of ∿ 1000 byte/sec). (5 FEMs in 1984 increasing to a maximum of approximately 20).

A virtual memory management system permitting all user programs at least 4 Mbyte of storage (program + data).

A File Management System with the following features:

a) A unified file structure such that files on the FEM and HUB computers are compatible.

b) The system should also provide monitor/restriction functions to a users available file space.

c) An archiving facility, new files should be automatically identified and copied to tape at pre-set time intervals.

d) The system should permit the production of non-standard formats on magnetic tape.

e) All sequential output devices shall have spooling facilitites.

A batch processing mode should be available.

ii) Network Software

iii) Data Base Software

An applications package which will keep track of the runs performed, their location within the various storage mediums and the analysis Performed on them.

iv) Users Applications Programs

7 Communications

The basic design requirements are:

a) That all terminals should be able to communicate with all processors In the PUNCH hierarchy above the one they are physically connected to.

b) File transfer should be possible between adjacent members of the hierarchy. It should be possible under (application) program control.

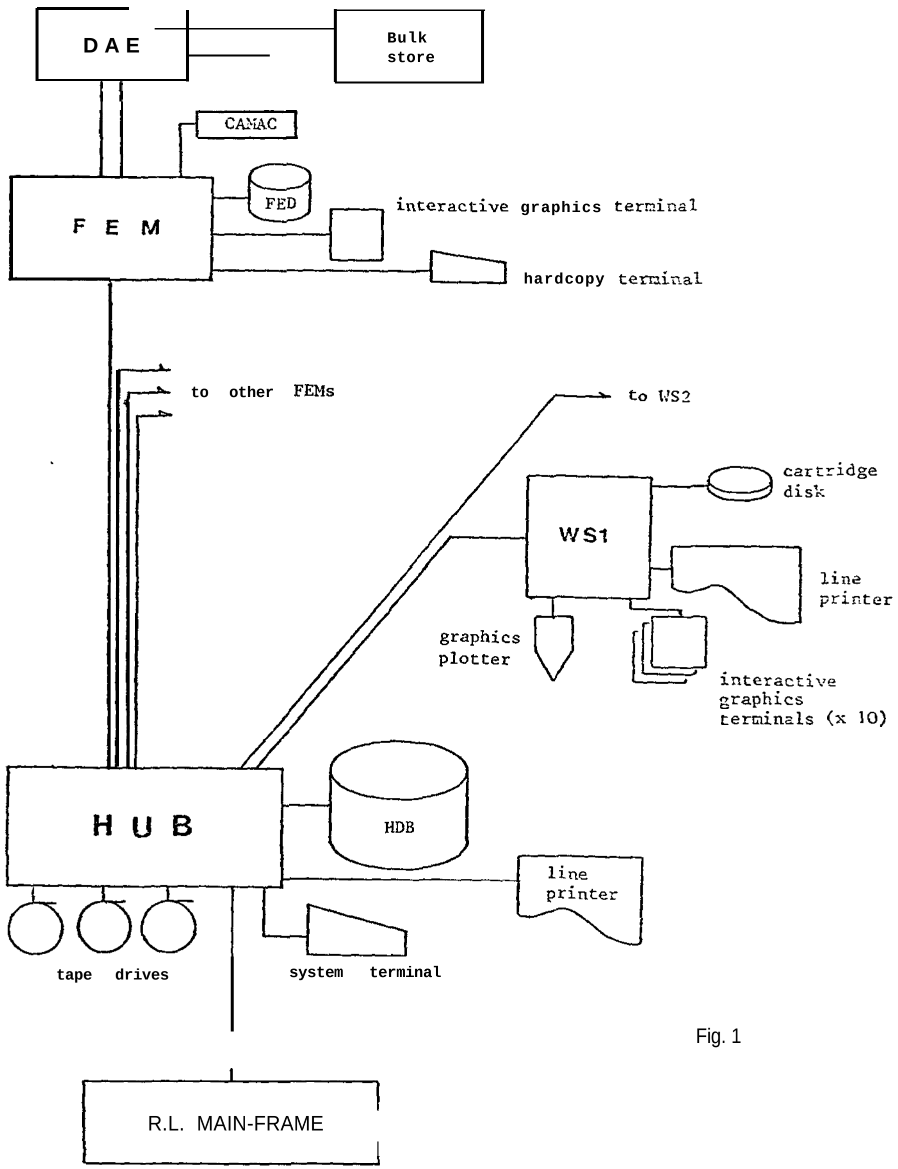
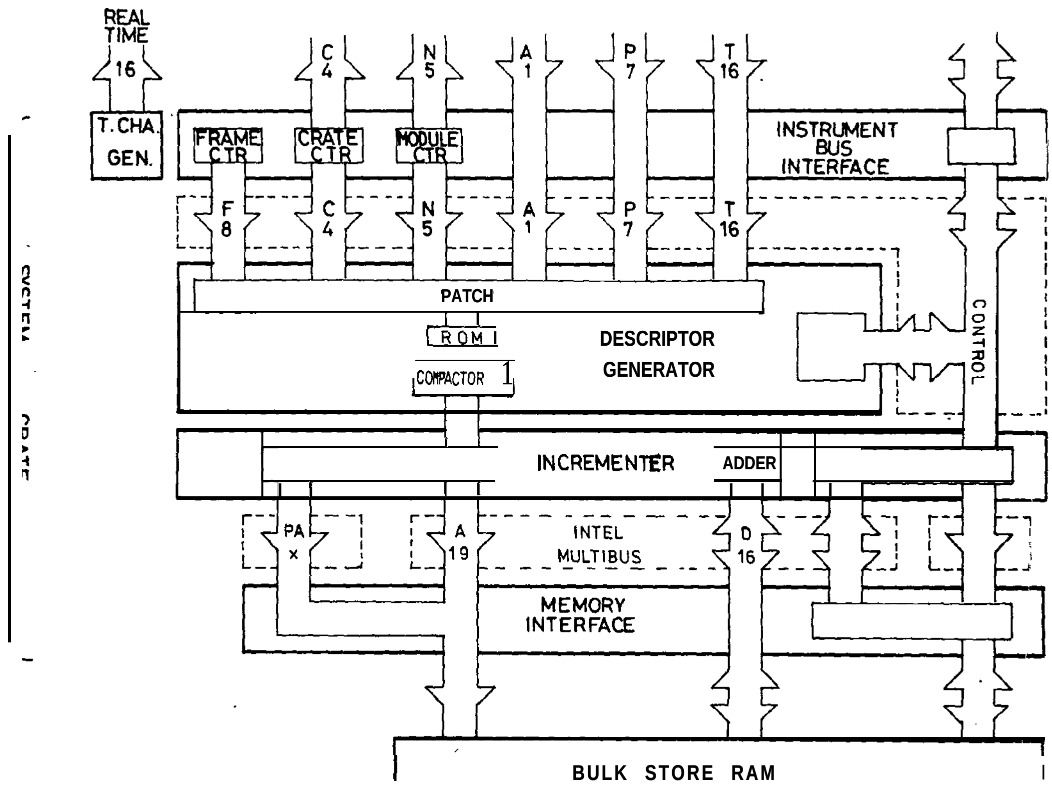
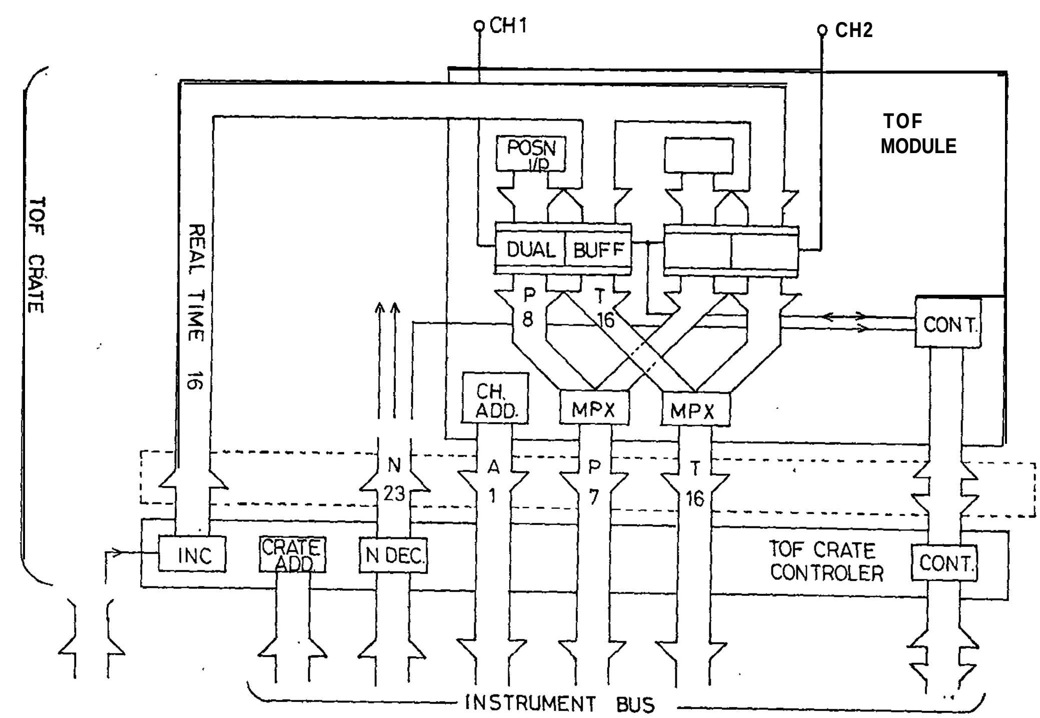


Fig. 1


REAL TIME
16
C 4
N 5
A 1
P 7
T 16
T.CHA. GEN.
FRAME CTR
CRATE CTR
MODULE CTR
INSTRUMENT BUS INTERFACE
F 8
C 4
N 5
A 1
P 7
T 16
PATCH
ROM
COMPACTOR
DESCRIPTOR GENERATOR
CONTROL
INCREMENTER
ADDER
PA x
A 19
INTEL MULTIBUS
D 16
MEMORY INTERFACE
BULK STORE RAM


CH1
CH2
TOF MODULE
POSN I/P
DUAL BUFF
P 8
T 16
CONT.
CH. ADD.
MPX
MPX
REAL TIME 16
TOF CRATE
N 23
A 1
P 7
T 16
INC
CRATE ADD
N DEC.
TOF CRATE CONTROLER
CONT.
INSTRUMENT BUS

(cont.)

Fig 2b